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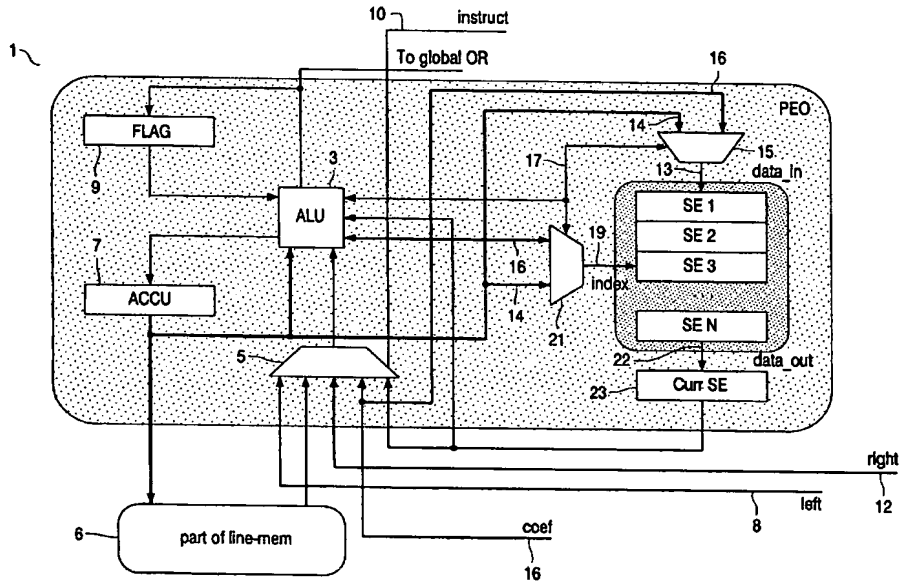
(54) Title: PARALLEL PROCESSING ARRAY



(57) Abstract: A processing element (1) forming part of a parallel processing array such as SIMD comprises an arithmetic logic unit (ALU) (3), a multiplexer (MUX) (5), an accumulator (ACCU) (7) and a flag register (FLAG) (9). The ALU is configured to operate on a common instruction received by all processing elements in the processing array. The processing element (1) further comprises a storage element (SE) (11), which supports the processing of local customized (i.e. data dependent) processing in the processing element (1), such as lookup table operations and the storing local coefficient data.

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